

### 2.6.3 Overflow

Under certain circumstances the result will be wrong! (Continuing with the 2's complement representation.)

#### Example 2.6.12

$$\begin{array}{r}
 0101 \quad (+5) \\
 +0011 \quad (+3) \\
 \hline
 1000 \quad (8) \text{ carry into MSB} \\
 \quad \quad \quad (sign \ change)??
 \end{array}$$


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#### Example 2.6.13

$$\begin{array}{r}
 0101 \quad (+5) \\
 +1011 \quad (-5) \\
 \hline
 (1)0000 \quad (0) \text{ carry into MSB + carry}
 \end{array}$$


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#### Example 2.6.14

$$\begin{array}{r}
 1011 \quad (-5) \\
 +1011 \quad (-5) \\
 \hline
 (1)0110 \quad (-10) \text{ no carry into MSB} \\
 \quad \quad \quad \text{but carry out of MSB ??}
 \end{array}$$


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These possible conditions need to be noted if errors are to be avoided.

- The carry bit is implemented as an extra bit used by the processor to record the carry(/borrow) out of the MSB's
- A further bit of information is noted by the processor to determine if an *overflow* or *underflow* condition has occurred. A simple rule is applied;