THE UNIVERSITY OF AUCKLAND

FIRST SEMESTER, 2008
Campus: City

COMPUTER SCIENCE
Advanced Computer Architecture
(Time Allowed: FIFTY minutes)

FAMILY NAME:
PERSONAL NAMES:
STUDENT IDENTIFICATION NUMBER:
LOGIN NAME:
SIGNATURE:

This test has 13 questions, all of equal value. Answer any three. If you answer more than three questions, the first three not crossed out will be graded.

Some questions are harder than others—they will be graded more generously.

Be concise. Long answers are not generally better answers.

QUESTION	MARKS	SCORE
	10	
	10	
	10	
TOTAL	30	

Continued...

Question 1

Compare and contrast DSTM and TL2. What are the most important differences? Which one do you think is better? Justify your answer.

Question 2

Explain the difference between visible and invisible reads. Is one more desirable than the other? If so, why isn't it always used? What circumstances favour visible reads and vice versa?

Question 3

What is wrong with locks? What is the appeal of transactional memory? Do you think it will catch on? Why or why not?

Question 4

Compare an STM designed for many threads to run concurrently against a lock-based system with coarse-grained locks. Assume both are running on a dedicated, single-processor system. Which would you expect to run faster? Why? That is, compare the overheads of the two systems.

Question 5

How well does DSTM scale? What limits its scalability? How well does TL2 scale? What limits its scalability? Which would you expect to perform better on a large number of processors? Which would expect to perform better on a single processor?

Question 6

What's the difference between atomicity and isolation. How does TM preserve both?

Question 7

Explain the difference between strong atomicity and weak atomicity.

Question 8

What is serializability? How does it relate to ACID?

Question 9

The basic algorithm used in NZSTM is blocking. What makes it blocking? How can it be made nonblocking?

Continued...

Question 10

What are the different possible levels of transactional granularity? Of the TMs we've covered, at what level do they operate? What's the advantages and disadvantages of each level?

Question 11

Explain how the cache coherence mechanism that makes possible efficient hardware support for transactional memory. What is the property that is being exploited?

Question 12

Show that it is possible to simulate Compare & Swap using Test & Set. Show that it is possible to simulate Test & Set using Compare & Swap. Is one of these mechanisms more powerful than the other? If not, explain. If so, why is the other ever implemented?

Question 13

The MOESI coherence protocol provides five states. The fifth state, Owned, is rarely implemented. A system is being designed where the Owned state will be used to provide an optional write-broadcast operation (instead of invalidate). The write-broadcast is optional, to be used only for certain kinds of write operations. Would you recommend using it for normal writes? Why or why not? Would your recommend using it for Test & Set? Why or why not? Would you recommend using it for Compare & Swap? Why or why not?

End of questions

Question #____

Question #____

Question #____