THE UNIVERSITY OF AUCKLAND

FIRST SEMESTER, 2005
Campus: City

COMPUTER SCIENCE

Advanced Computer Architecture

(Time Allowed: NINETY minutes)

FAMILY NAME:
PERSONAL NAMES:
STUDENT IDENTIFICATION NUMBER
LOGIN NAME
SIGNATURE

This test has a maximum score of 40 possible Marks. It has a total of 7 questions, and you should try to answer all of them.

Write your answers in the places provided in this booklet. Show your work for partial credit..

QUESTION	MARKS	SCORE
A.1	6	
A.2	6	
A.3	6	
A.4	6	
A.5	5	
A.6	6	
A.7	5	
TOTAL	40	

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Question A.1 6 Marks

The binary n-cube, or Hypercube, is an expandable topology that offers extreme regularity and simple routing.

(a) Draw a picture of a 4-dimensional hypercube and assign numbers to the nodes.

(b) How many nodes are there in a 6-dimensional hypercube?

(c) How many links are there in a 6-dimensional hypercube?

(d) What is the maximum distance between any pair of nodes in a 6-dimensional hypercube?

(e) What is the average distance between any pair of nodes in a k-dimensional hypercube? (Hint: assume a node communicates with every other node, including itself.)

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Question A.2 6 Marks

After pipelining was introduced into microprocessors, the use of microprogamming as an implementation technique largely disappeared, except for architectures already in use.

(a) How would you characterize instructions defined for a microprogrammed computer?

(b) Explain the difficulties in designing a pipelined implementation of an instruction set designed for a microprogrammed computer.

(c) How can such difficulties be overcome/handled?

Question A.3 6 Marks

Wulf' s paper, "Compilers and computer architecture," appeared in 1981, before the first commercial "RISC" processors appeared. Did the designers of those architectures (e.g., MIPS & Alpha) follow Wulf' s advice?

(a) Did they provide instruction sets that were regular, orthogonal, and composable? Support your answer with an example.

(b) Did they provide instruction sets that provided good run-time environments for programs? Support your answer with an example.

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Question A.4 6 Marks

Wang, Baer, and Levy concluded that a multilevel cache system supporting multiprocessing should maintain multi-level inclusion. Jouppi described a victim cache that explicitly did not include multi-level inclusion.

(a) Explain what is meant by multi-level inclusion.

(b) What is the value of multi-level inclusion?

(b) Are these proposals consistent? Explain why or why not. Specifically, explain how the benefits of multilevel inclusion are obtained or unneeded for a victim cache.

Question A.5 5 Marks

Suppose that you have come up with a scheme that allows the compiler to convey information along with each branch instruction, allowing the hardware to predict *all* branches correctly.

Would this solve the bottleneck of control flow? If not, what problems would need to be solved to exploit this prediction capability most effectively.

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Question A.6 6 Marks

Early microprocessors supported floating point instructions with a separate floating-point chip that extended the instruction set. If the chip was not present, the computer encountering these instructions would take an "unimplemented instruction" exception. A software routine could then be supplied, allowing the "execution" of the instruction through a software library of instructions.

Assume that on average, each floating point instruction executed on the floating-point chip took 3 times as long to execute as the average of all non-floating-point instructions. Assume also that the software interpretation of a floating-point instruction requires the execution of 7000 instructions.

What is the speed-up achieved by adding the floating-point chip for a program for which the percentage of instructions that must be thus emulated is

(a) .001%

(b) 1%

(c) 50%

Question A.7 5 Marks

SimpleScalar actually is two separate simulators, (1) a functional simulator that determines the effect of executing an instruction and (2) a timing simulator that determines the time (in clock cycles) to execute the program on a specific implementation. Simulations can be classified as time-based, event-based, or process-based. Are these simulators time-based, event-based, or process-based? Explain.

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