Project Requirements

- Proposal (due: Friday, May 5)
- Final Proposal (due: Friday, May 12)
- Progress report: (Tuesday, May 23)
- Final Project (due: Friday, June 2)

Proposal

Preliminary: Due Friday 5May06 *Final: due Friday 12May06*

- Proposals may be turned in earlier to get earlier feedback. Feel free to come and talk with me during my office hours or by appointment.
- Proposal should be 1-2 pages long. It should include:
  - A description of your topic
  - A statement of why you think the topic is interesting or important, (for projects with original research) a description of the methods you will use to evaluate your ideas, and
  - References to at least three papers you have obtained. (The text and the papers we've read point to many papers. See also Proceedings of ISCA, HPCA, ASPLOS, IEEE Transactions on Computers, ACM Transactions on Computer Systems, IEEE Computer, IEEE Micro, IEEE Transactions on Parallel and Distributed Systems.)
- Come see me to talk about ideas and possibilities
- Ideas for projects on Assignments web page.

Progress Report

Progress Reports should include a revised version of the proposal plus one page describing accomplishments so far. Concentrate on describing sub-tasks completed, rather than the tasks started. For example, say "completed simulator design at subroutine level" rather than saying "started writing simulator".

Description of Project

A project related to Computer Architecture

- A survey of a research area
  - Held to a higher standard
  - Must read and report on a minimum of three papers beyond those assigned in class. I expect that at least one paper would come from a recent ISCA, MICRO, HPCA or ASPLOS
  - Summarize the state-of-the-art in some area, describing controversies and alternative proposals
- A project involving simulation or other analysis
  - May be a group project
  - Replicate results reported in (quality) published paper
  - Evaluate new ideas

Project Topics

- Experimentally reproduce results from any recent architecture research paper
- Cache coherence: buses or point-to-point links?
- Comparison of two (or more) specific cache coherence protocols
- Compare two (or more) latency tolerating techniques.
- Evaluate the benefits of out-of-order execution
- Study cache parameters: size, associativity, block size, write policy, ...
- Evaluate the effect on cache hierarchies of multi-core processors on-chip

Survey Topics

- Chip multiprocessing and cache organization
- Interconnects for chip multiprocessing
- Synchronization Primitives
- Hybrid HW/SW Transactional Memory
- Trade-offs in interconnect or network routers
- Methods for increasing reliability, availability, or serviceability of parallel systems
- Hardware support for debugging parallel programs

Possible Topics for Survey

The current state of

- Transactional Memory
- Snooping cache protocols
- Directory-based caches
- Synchronization primities
- Speculative multithreading
- Memory hierarchies
- CMPs
- Particular approaches to ILP

More Survey Topics

- How does chip multiprocessing (CMP) change coherence tradeoffs?
- Will Chip Multiprocessor (CMP) L1 cache stay write-through?
- Will CMP L2 caches stay shared?
- Will CMP affect how to do synchronization?
- Ways of using multi-threading capability to support a single thread of execution
- Will future chips be CMPs, Simultaneous Multithreaded (SMTs), both, or neither?
- Trace the evoluation of Cray architectures, including the XMP, T3D, T3E, and X1.
- Compare the directory protocols of the SGI Origin2000 and Compaq GS320

Still More Survey Topics

- Should CMPs use buses, crossbars, or other interconnects?
- Study tradeoffs in interconnect or network routers.
- Compare successive processors in a given series (MIPS, Intel, Cray, Alpha, etc.)
- Why might SIMD or data parallel rise again?
- Study methods of increase reliability, availability, or serviceability of parallel systems.