DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
The University of Auckland
COMPSYS 304 / COMPSCI 313
Computer Architecture
Semester 2, 2012

Lecturers:

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Course coordinator: Dr. Morteza Biglari-Abhari

Course learning outcomes:

Students will be able to:

- understand the basics of modern computer architectures and quantitative principles of computer design in order develop a conceptual understanding of issues involved in designing a high performance computer system
- design and evaluate the instruction set architectures (both RISC and CISC) and how it can be related to the hardware/software interface in a computer system with a quick review in assembly programming
- understand different processor implementation methods including the basic single-cycle implementation and how it can be extended to a multi-cycle, pipelined and superscalar implementations
- understand performance evaluation techniques and their relation to the target applications and the processor work load
- understand the memory hierarchy in a modern computer system and its impact on the performance of the system. This includes physical and virtual memory systems and basics of cache memories.
- understand some basic principles of parallel computing as special topics in this course (more advanced materials for this part will be covered in a more advanced postgraduate level course)
- use and apply this knowledge to select computers for specific tasks. This course will give you an understanding of the effects of design decisions on performance and make you a well-informed consumer in addition to a processor designer.

Assessment:

Three assignments and one test in addition to the final exam are used to assess students' achievements related to the learning outcomes. The first assignment is mainly on the instruction set architecture design, hardware/software interfacing and review of assembly programming and issues in processor implementation. The second assignment is related to processor implementation and performance issues. The third assignment will be related to memory hierarchy system and multiprocessing.
The test and final exams will assess all parts of the learning outcomes.

Assignment 1:	4%	due Mon. 6 August
Assignment 2:	4%	due Mon. 10 September
Assignment 3:	7%	due Thu. 11 October
Test:	15%	(in Week 6 or Week 7)

Recommended textbook:

- David A. Patterson and John L. Hennessy, Computer Organization and Design: The Hardware/Software Interface, Fourth Edition, 4th ed, 2009 by Elsevier/Morgan Kaufmann Publishers (or 3rd ed.)

- Lecture notes may be provided on Cecil

Academic integrity notice:

The University of Auckland will not tolerate cheating, or assisting others to cheat, and views cheating in coursework as a serious offence. The work that a student submits for grading must be the student's own work, reflecting his or her learning. Where work from other sources is used, it must be properly acknowledged and referenced. This requirement also applies to sources on the world-wide web. A student's assessed work may be reviewed against electronic source material using computerised detection mechanisms. Upon reasonable request, students may be required to provide an electronic version of their work for computerised review.