

Computer Science 210  
Computer Systems 1  
Lecture Notes

Lecture 8  
**Sequential Logic &  
Finite State Machines**

Credits: Slides adapted from Gregory T. Byrd, North Carolina State University

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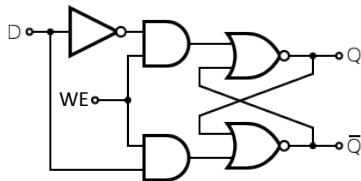
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### Gated D-Latch

Two inputs: D (data) and WE (write enable)

- when **WE = 1**, latch is set to value of D
  - $S = D$ ,  $R = \text{NOT}(D)$
- when **WE = 0**, latch holds previous value
  - $S = R = 0$



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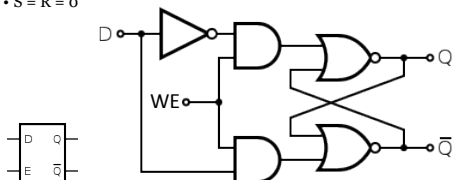
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Symbol for a Gated D-Latch

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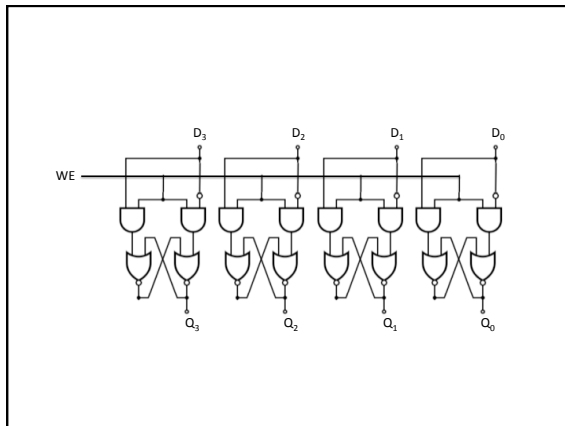
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## Representing Multi-bit Values

Number bits from right (0) to left (n-1)  
– a convention

Use brackets to denote range:

**D[l:r]** denotes bit **l** to bit **r**, from *left to right*

$A = \overset{15}{0} \overset{14}{1} \overset{13}{0} \overset{12}{0} \overset{11}{0} \overset{10}{1} \overset{9}{1} \overset{8}{1} \overset{7}{0} \overset{6}{1} \overset{5}{0} \overset{4}{1} \overset{3}{0} \overset{2}{1} \overset{1}{0} \overset{0}{1}$   
 $A[14:9] = 101001$        $A[2:0] = 101$

• May also see  $A\langle 14:9 \rangle$ ,  
especially in hardware block diagrams.

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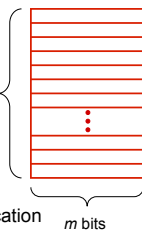
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## Memory

Now that we know how to store bits,  
we can build a memory – a logical  $k \times m$  array of  
stored bits.

**Address Space:**  
number of locations  
(usually a power of 2)

$k = 2^n$   
locations



**Addressability:**  
number of bits per location  
(e.g., byte-addressable)

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6

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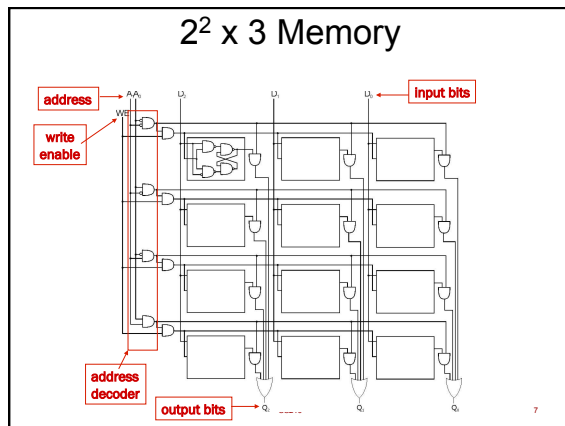
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## More Memory Details

This is a simplification

- fewer transistors, much more dense, relies on electrical properties

• But the logical structure is very similar:

- address decoder
- select register
- word write enable

Two basic kinds of **RAM** (Random Access Memory)

- **Static RAM (SRAM)**

- fast, maintains data as long as power applied

- **Dynamic RAM (DRAM)**

- slower but denser, bit storage decays – must be periodically refreshed

Also, non-volatile memories: ROM, PROM, flash, ...

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8

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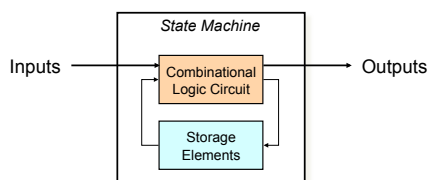
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## State Machine

Another type of sequential circuit

- Combines combinational logic with storage
- “Remembers” state, and changes output (and state) based on **inputs** and **current state**



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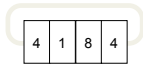
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## Combinational vs. Sequential

- Two types of “combination” locks



### Combinational

Success depends only on the **values**, not the order in which they are set.



### Sequential

Success depends on the **sequence** of values (e.g., R-13, L-22, R-3).

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10

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## State

The **state** of a system is a **snapshot** of **all the relevant elements** of the system at the moment the snapshot is taken.

- Examples:

- The state of a tic-tac-toe (Noughts & Crosses) game can be represented by the placement of X's and O's on the board.
- The state of a cricket game can be represented by the scoreboard
  - Number of runs & wickets, overs remaining, etc.

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11

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## State of a Turnstile

The turnstile has 2 states

- locked** and **unlocked**

The turnstile has 2 inputs

- putting in a coin (**coin**)
- pushing the bar (**push**)



Current State	Input	Next State	Output
Locked	coin	Unlocked	Release turnstile so customer can push through
	push	Locked	None
Unlocked	coin	Unlocked	None
	push	Locked	When customer has pushed through lock turnstile

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12

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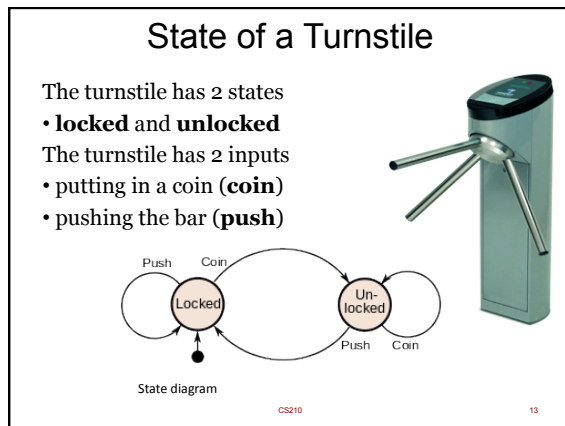
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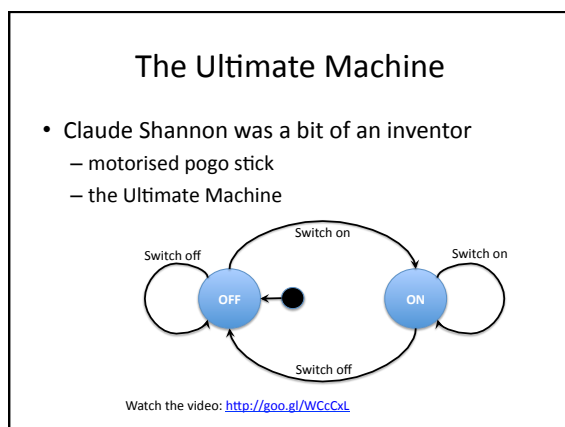
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