

Computer Science 210  
Computer Systems 1  
Lecture Notes

Lecture 7  
**Digital Logic Structures**

Credits: Slides prepared by Gregory T. Byrd, North Carolina State University

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## Building Functions from Logic Gates

**Combinational Logic Circuit**

- output depends only on the current inputs
- stateless

**Sequential Logic Circuit**

- output depends on the sequence of inputs (past and present)
- stores information (state) from past inputs

We'll first look at some useful combinational circuits, then show how to use sequential circuits to store information.

CS210 2

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## Decoder

**n inputs,  $2^n$  outputs**

- exactly one output is 1 (true) for each possible input pattern

**2-bit decoder**

Can detect a pattern in a string of input bits – can have any number of inputs

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**Two Variables**  
16 possible unique functions

A	B	f <sub>0</sub>	f <sub>1</sub>	f <sub>2</sub>	f <sub>3</sub>	f <sub>4</sub>	f <sub>5</sub>	f <sub>6</sub>	f <sub>7</sub>	f <sub>8</sub>	f <sub>9</sub>	f <sub>10</sub>	f <sub>11</sub>	f <sub>12</sub>	f <sub>13</sub>	f <sub>14</sub>	f <sub>15</sub>
0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
0	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	1
1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

$\overline{A \vee B} = \overline{A} \wedge \overline{B}$   
 NOR  
 De Morgan's Law

$\overline{A \wedge B}$   
 NAND

$A \wedge B$   
 AND

$A \wedge B$   
 AVB

$A \wedge B$   
 AVB

$A \wedge B$   
 XNOR

$A \wedge B$   
 AVB

$A \wedge B$   
 OR

$A \wedge B$   
 AVB

CS210 4

**Truth Table for Function F**

A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

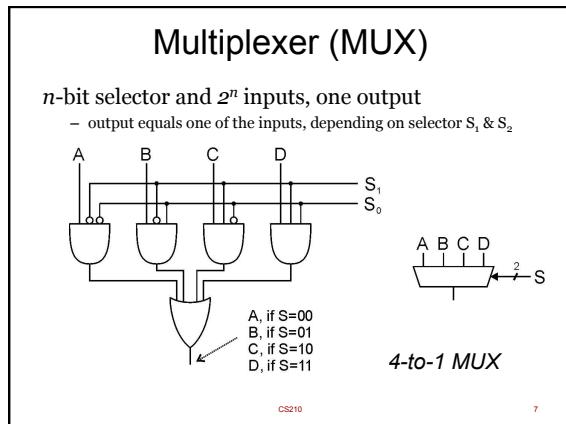
XOR  
 F is True if 1 or 3 inputs are true  
 F is False if zero or 2 inputs are true  
 More generally F is true if an odd number of inputs are true

CS210 5

**Creating a Circuit from a Truth Table**

A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

CS210 6




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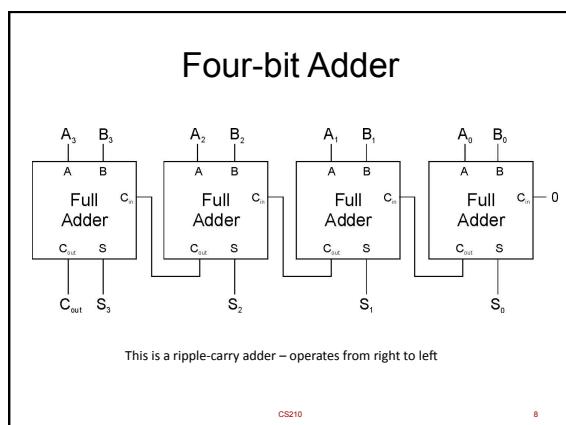
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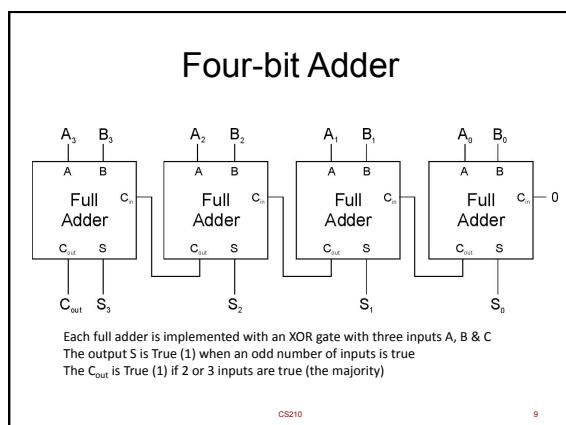
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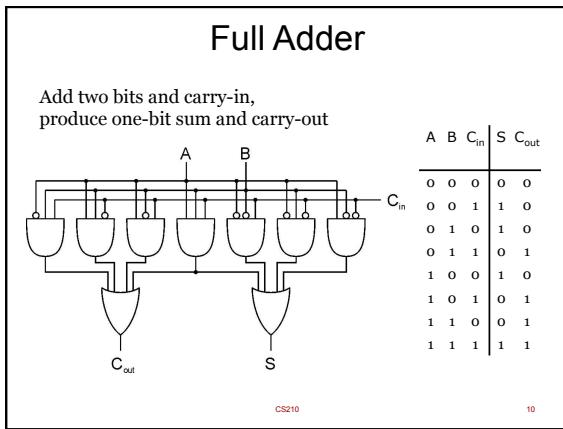
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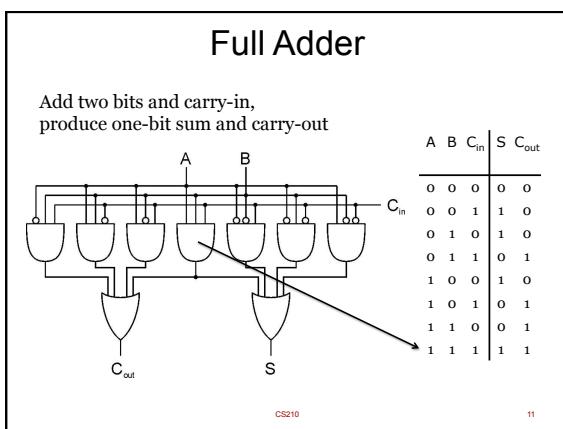
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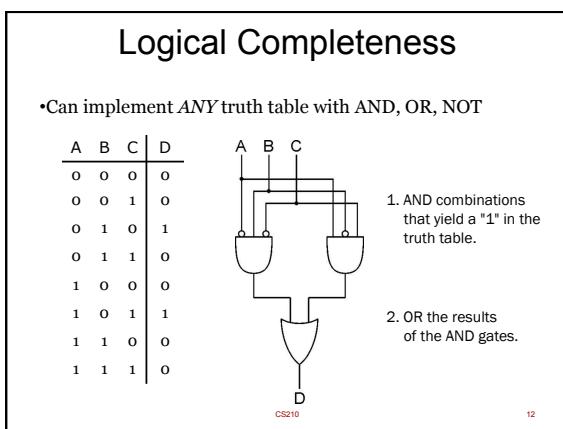
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## Logical Completeness

A	B	C	D
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

Can implement *ANY* truth table with just NAND or NOR

We might not want to for reasons of simplicity

CS210

13

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## DeMorgan's Law

$$\begin{array}{lcl} \text{NAND gate} & = & \text{Inverter} \\ \text{Inverter} & = & \text{NOR gate} \end{array}$$

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14

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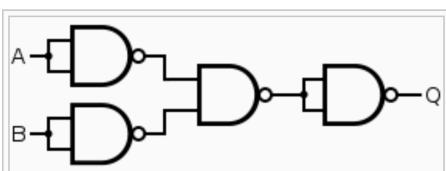
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## De Morgan's Theorem

Using Only NAND gates to create a NOR gate



NOR gate constructed using only NAND gates

credit: [http://en.wikipedia.org/wiki/NOR\\_gate](http://en.wikipedia.org/wiki/NOR_gate)

CS210

15

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### De Morgan's Theorem

Using Only NOR gates to create a NAND gate

NAND gate constructed using only NOR gates

credit: [http://en.wikipedia.org/wiki/NOR\\_gate](http://en.wikipedia.org/wiki/NOR_gate)

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### Combinational vs. Sequential

**Combinational Circuit**

- always gives the same output for a given set of inputs
  - ex: adder always generates sum and carry, regardless of previous inputs

**Sequential Circuit**

- stores information
- output depends on stored information (state) plus input
  - so a given input might produce different outputs, depending on the stored information
- *example:* ticket counter
  - advances when you push the button
  - output depends on previous state
- useful for building "memory" elements and "state machines"

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17

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### SR-Latch: Simple Storage Element Flip-Flop

S is used to "set" the element – set output Q to one  
R is used to "reset" or "clear" the element – set output Q to zero

NAND SR-Latch

S	R	Action
0	0	Restricted combination
0	1	Q = 1
1	0	Q = 0
1	1	No Change

This gives us the ability to store a bit (either 0 or 1)

Watch the video <http://youtu.be/n5jD7Q7BSA>

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18

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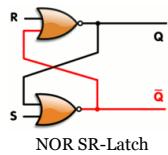


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### SR-Latch: Simple Storage Element Flip-Flop

S is used to "set" the element – set output Q to one

R is used to "reset" or "clear" the element – set output Q to zero



Characteristic table			
S	R	$Q_{next}$	Action
0	0	Q	hold state
0	1	0	reset
1	0	1	set
1	1	X	not allowed

This gives us the ability to store a bit (either 0 or 1)