

Mini-assignment 2 is not yet ready. The due date (originally 3April) will be deferred until after the break. ldq Reg, Address ! Direct

What's the problem?

- Address is stored as a constant inside the instruction

 How to *dynamically* change the address?
- Instructions should be small, fixed size
 - Addresses are large
 - How to store a 51-bit address in a 32-bit instruction?
- Also a problem for branch instructions:

bne Reg, Address

Load/Store Instructions			Idea: Add another word				
Load/Store ^{6 bits} • How to sp <i>address</i>)		21 bits nory address (<i>effective</i> y 21 bits?		• Load • 21 + But • Instr			
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Idea 2: Address is in Register

- Load instruction specifies a register to supply address: Register Indirect
- Easy to change address without changing instruction But
- How does the address get into the register?
- How is the address modified?

Idea 3: Construct Effective Address

- Ida instruction loads constant into register Ida reg, constant
- Can adjust address dynamically (using addition)
- 21-bit constant is not big enough
- Assume <constant> is 32 bits
- Break <constant> into two 16-bit pieces:
 16 most significant bits: <hi address>
 16 least-significant bits: <low address>

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Idea 3: Construct Effective Address

• Use instruction sequence:

lda \$8, <hi address>
sll \$8, \$8, 16
lda \$9, <low address>
bis \$8, \$9, \$10 ! Logical OR
ldq \$11, (\$10) ! Register indirect

- Five instructions!
- Variant: use add instead of OR
 - sign-extend <low address> add \$8, \$9, \$10 ! Instead of Logical OR
 - Doesn't quite work if <low address> is negative!

Optimization: Ida, Idah

lda	Reg A	Reg B	<low address=""></low>
6 bits	5 bits	5 bits	16 bits
ldah	Reg A	Reg B	<hi address=""></hi>
6 bits	5 bits	5 bits	16 bits

- lda A, <low address>(B)
 - sign-extend constant <lowaddress> and add to contents of register
 B; assign result to register A
- ldah A, <hi address>(B)
 - multiply constant <hi address> by 65,536 and add to contents of register B; assign result to register A

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- Usually only requires 2 instructions
 - Still only generates 32-bit addresses
 - Some 32-bit integers cannot be generated this way

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Locality of Reference

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Observation: memory references are not random

- Accesses tend to be clustered
 - in time (temporal locality)
 - in space (spatial locality)
- Accesses are to objects
 - structures
 - arrays
- Can dynamic compute address arithmetically
- Can statically predict offset within known structure

Idea 4: Use Combination

- Base + Displacement
- Base: a long-term but approximate address
 - Gives location of larger structure
 - Can be dynamically varied
- Displacement
 - Static offset embedded in instruction
 - Cannot be dynamically varied

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Load Reg, Disp(Base)					Special Case of Base + Displacement			
Idq 6 bits	Dest 5 bits	Base 5 bits	Displacement 16 bits	 Register Direct Zero displacement Register specifies address 				
 Effective address: (Base) + Displacement Base is a 64-bit address Displacement is a 16-bit signed constant, sign-extended to 64 bits Displacement defines position <i>relative to</i> Base 				ed				
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