SIGNAL DELAY IN RC TREES WITH CHARGE SHARING OR LEAKAGE

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ABSTRACT

A single value for delay, based upon the delay of Elmore, is derived for two types of RC tree networks. In one type of network, there is no driving source: this undriven situation causes static charge sharing among nodes. An expression for delay is obtained by straightforward analysis of this network.

In our second case, an RC tree which is driven by at least one source has leaky capacitors. We show how to calculate delays for such trees by a linear time algorithm.

A simple MOS circuit with a leakage path to ground is analyzed using the method presented in this paper. The result is compared with that of SPICE.

1. Introduction

Modeling digital MOS circuits by RC networks for the purpose of estimating delay has become a well accepted practice [9,11,12,4,7]. One approach pioneered by Rubinstein, Penfield and Horowitz (R-P-H) is to model a circuit as an RC network driven by a single source [9,11,12,4]. Crystal [7] takes a more restrictive approach, calculating the delay at a node by considering only a single resistive path to the source.

The result of a delay calculation may be a single value [7], a "best fit" exponential [4], or a pair of bounding waveforms [9,11,12]. We choose the intermediate course of supplying a "best fit" exponential.

The RC model of R-P-H [9] depends on two basic approximations. Transistor inputs are approximated by step waveforms, and conducting transistors are approximated by linear resistors. A simulation program like SPICE [5], on the other hand, makes no such approximations and is hence computationally much slower, though more accurate. The R-P-H approach is conceptually simple and computationally efficient, and has been incorporated into several timing-analysis programs [3,10]. In this paper, we employ this basic R-P-H model.

Most analyses of RC networks introduce several additional assumptions. One is that all RC networks need to be driven by exactly one source. However, many MOS circuits used in practice have no driving source: this undriven situation may cause static charge sharing among nodes [1], a situation we have addressed in this paper. Secondly, there are instances where more than one source drives a network. For example, consider an nMOS inverter driving two loads with its input set to logic value '1'. The load capacitors are driven by two sources, VDD and GND. To the best of our knowledge, ours is the only analysis to allow multiple sources. A third additional assumption of analyses of RC networks is that all capacitors are ideal, having no leakage path to ground. Under this assumption, a previously charged capacitor that is isolated from the rest of the circuit would retain its charge for an infinite duration of time. Yu and Wyatt [12] relax this assumption, allowing one leaky capacitor. Our analysis permits any number of leaky capacitors.

A fourth additional assumption that many models make is that the RC network is a tree, meaning that no resistor meshes are allowed. Lin and Mead (L-M) [4] have provided a "best fit" exponential for an RC mesh. Wyatt [11] extends this, providing a pair of bounding waveforms for an RC mesh. In this paper, we analyze the restricted case of an RC tree.

A most general RC model would allow floating capacitors in the network. No floating capacitors are permitted in this paper. There exists no known analysis for such a model, and it remains an important open problem for future research.

The proofs of all theorems in this paper can be found in [8].

2. The Timing Model

The timing model for MOS transistor circuits is based on the switch model proposed by Bryant [1]. In this model, a circuit is represented by a set of transistors $\{t_1, ..., t_m\}$ and a set of nodes $\{p_1, ..., p_n\}$. With each node p_i are associated a resistance, a capacitance, a charge and a voltage source. Also associated with a node is a state, which is a function of its charge. With each transistor are associated a set of resistances. The value of a transistor's resistance depends on the the state of the node controlling its gate and on the states of its other two nodes, the source and the drain. Although the capacitance and resistance at a node and the resistance of a transistor are voltage dependent, they are assumed as constants here.

The evolution of an MOS circuit is approximated by a sequence of RC networks. Various node capacitors are charged and discharged through the network. This charging-discharging process may change the state of a node which in turn changes the topology of the RC network. The process continues until the topology of the network changes no longer.

Definition 1. An RC network is a loopless connected graph on n nodes. With each edge i is associated a nonnegative resistance r_i. With each node k are associated a positive resistance R_k, a positive capacitance C_k, a nonnegative charge Q_k and a voltage source $v_k \in \{VDD, GND, \phi\}$, where ϕ indicates no connection.

Circuit elements associated with a node in the definition are elements that exist between the node and GND in the network. Note that this definition does not allow for floating capacitors (capacitors associated with the edges of the graph) in the network.

When the edges and nodes are all labeled with numbers, these parameters can be grouped together as vectors. An RC network is then denoted by $N(n, r, R, C, Q, V)$, where n is the number of nodes, r is a vector of edge resistances, R is a vector of leakage resistances, C is a vector of node capacitances, Q is a vector of capacitance charges, and V is a vector of node voltage sources. In Fig. 1, below, the nodes are labeled by circled indices. Edges are the series resistors r_i. A single leakage resistor, R_3, is shown. All other leakage resistors are (by default) infinite.
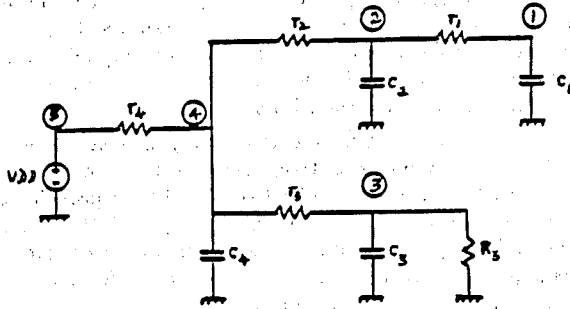

Figure 1. A standard RC network.

With the approximations introduced above, the problem of estimating the delay of an MOS circuit reduces to that of estimating the delay of an RC network. Certain special cases of RC networks, which occur in this paper, are denoted below:

1) $N(n, r, R, C, Q, VDD_n)$: An RC network with n nodes, driven by a single source, namely VDD, which is connected to node n. This network will be referred to as the standard network, or N_n, in the rest of the paper. Fig. 1 is an example of N_5.

2) $N(n, r, R, C, Q, GND_n)$: The same network as in 1) with node n connected to GND.

3) $N(n, r, \infty, C, Q, \phi)$: An RC network on n nodes with only ideal capacitances and no sources. This network will be referred to as the charge sharing network, or $N_n(\phi)$ in the rest of the paper.

Since our RC networks are loopless, we may assign the label $\min(a, b)$ to the edge (a, b).

Define a path nk to be the (unique) list of edges joining node n to node k. Let $R_{k,i}$ denote the sum of the resistances of the edges common to the unique paths nk and ni [9]. For example, in Fig. 1, $R_{2,2} = r_4 + r_2$ and $R_{2,3} = r_4$. Note that a doubly subscripted $R_{k,i}$ is distinct from a leakage resistance R_k.

3. Definition of Delay

Prior to analysis, it is necessary to have a consistent and unambiguous definition of delay. Although there are a number of such definitions in practical use, most of these are awkward for theoretical investigation. Accordingly, we define delay as

$$\tau = \frac{\int_0^\infty [v(\infty) - v(t)]\, dt}{v(\infty) - v(0)}. \tag{1}$$

We now have a "best fit" exponential waveform with time constant τ_i,

$$\bar{v}_i(t) = v_i(0) + [v_i(\infty) - v_i(0)](1 - e^{-t/\tau_i}) \tag{2}$$

where $v_i(t)$ represents the voltage waveform at node i.

Theorem 1. $\bar{v}_i(t)$ satisfies the property

$$\int_0^\infty (v_i(t) - \bar{v}_i(t))\,dt = 0 \tag{3}$$

Definition 2. The parameter D_i is defined as the product of $(v_i(\infty) - v_i(0))$ and the delay τ_i.

$$D_i = (v_i(\infty) - v_i(0)) \cdot \tau_i \tag{4}$$

When the context is not obvious, we will refer to D_i in a network $N(n, r, R, C, Q, V)$ as $D_i(n, r, R, C, Q, V)$. As the next few theorems show, most of our results on delay are expressed through the parameter D_i.

We need another important result from network theory, the **Superposition Theorem** [2], which can be stated as follows for the purpose of this paper.

Theorem 2. $D_i(n, r, R, C, Q, V)$ is obtained as the sum of the D_i in each network obtained from $N(n, r, R, C, Q, V)$ by setting all but one source to GND.

$$D_i(n,r,R,C,Q,V) = D_i(n,r,R,C,Q,[v_1]) \tag{5}$$
$$+ D_i(n,r,R,C,Q,[v_2])$$
$$+ \cdots$$
$$+ D_i(n,r,R,C,Q,[v_n]).$$

where $[v_i]$ represents the vector V with all sources $\in \{VDD\}$ other than v_i set to GND.

Theorem 3. $D_i(n, r, R, C, Q, GND_n)$ is obtained as the difference between the D_i in the networks N_n (the same network, but driven by VDD at node n), and $N_n(0)$ (the standard network with no initial charge).

$$D_i(n,r,R,C,Q,GND_n) = D_i(n,r,R,C,Q,VDD_n) \tag{6}$$
$$- D_i(n,r,R,C,0,VDD_n)$$

where the network $N(n, r, R, C, 0, VDD_n)$ represents the standard network N_n with the capacitances having no initial charge.

Theorem 4. (The discharging theorem.) Let Q represent the final charge attained by $N(n, r, R, C, 0, VDD_n)$. The delay at node i in network $N(n, r, R, C, Q, GND_n)$, is the same as the delay at node i in the network $N(n, r, R, C, 0, VDD_n)$.

A consequence of theorems 2 & 3 is that we need an expression for delay only in the charge sharing and standard networks.

4. An Expression for Delay in the Charge Sharing Network

Consider a charge sharing network with n nodes, $N_n(\phi)$. We need to derive an expression for delay at some node in the network. Renumber the nodes as follows: the node for which we need to solve is numbered n, and the other nodes are numbered by a depth first traversal of the tree.

The final voltage at any node i in the network is obtained as

$$v_i(t) = \frac{\sum_{i=1}^{n} Q_i}{\sum_{i=1}^{n} C_i} \qquad (7)$$

Here, the Q_i stand for the charge in C_i at time $t=0$.
Kirchoff's voltage law and charge conservation give the expression for delay at node n as

$$\tau_n = -\frac{\sum_{i=1}^{n-1} C_i \sum_{k=1}^{n-1} R_{k,i} C_k (v_k(\infty) - v_k(0))}{(v_n(\infty) - v_n(0)) \sum_{k=1}^{n} C_k} \qquad (8)$$

Naive evaluation of this expression takes $O(n^2)$ time, but it can be done in $O(n)$ time by taking advantage of the tree structure of $R_{k,i}$.

5. An Expression for Delay in the Standard Network

Prior to any further discussion, a more constructive definition of standard RC networks than the one provided in Sections 1 & 2 is given. A standard RC network is recursively defined to be one of the following:

a) A resistor in series with a nonideal capacitor. The free end of the resistor is the input, labeled 2, and its other end is the output, labeled 1. The other end of the capacitor is grounded. This is shown in Fig. 2(a). This network will also be referred to as the primitive element or N_2 in the rest of the paper.

b) A series connection of the primitive element and an RC network with n nodes, N_n, to give N_{n+1}. The input of N_{n+1} is the input of N_2, with the input of N_n connected to the output of N_2. The nodes in N_{n+1} are renumbered as follows: The node numbers in N_n remain unchanged. Node 2 of N_2 is relabeled $n+1$. This is shown in Fig. 2(b).

c) A parallel composition of an n-node network N_n with an m-node network N_m, forming a network N_{n+m-1}. The input of N_{n+m-1} is the input of N_n, as shown in Fig. 2(c). The nodes in N_{n+m-1} are renumbered as follows: The node numbers in one of them, say N_n, remain the same except for the input node, while the node numbers in N_m get incremented by $n-1$. The input node of N_{n+m-1} gets the label $n+m-1$.

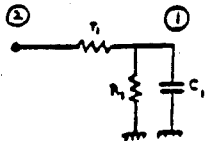In all three cases, the input node is connected to VDD.
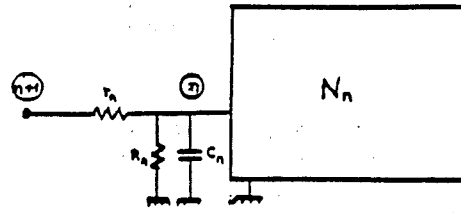

Figure 2(a). The primitive network N_2.

Figure 2(b). Series composition.

Having defined standard RC networks as dealt with in this paper, we recursively define certain parameters associated with such a network. Their circuit interpretation can be found in [8].
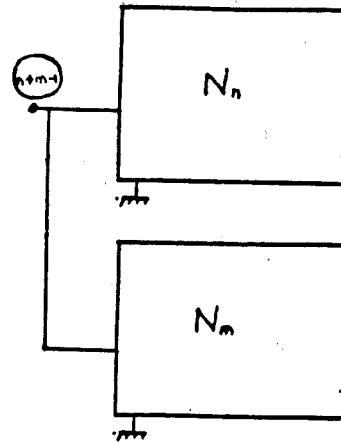

Figure 2(c). Parallel composition.

Theorem 5(a). For the primitive element N_2 (see Fig. 2(a)), the various parameters are given by

$$\rho^{(2)} = r_1 + R_1$$

$$v_1^{(2)}(\infty) = \text{VDD} \cdot \left[\frac{R_1}{r_1 + R_1}\right]$$

$$\overline{C}^{(2)} = \text{VDD} \cdot \left[\frac{R_1}{r_1 + R_1}\right] \cdot C_1$$

$$Q^{(2)} = v_1(0) \cdot C_1$$

$$(R_1^{~})^{(2)} = \frac{R_1}{r_1 + R_1}$$

$$\sigma^{(2)} = \frac{1}{r_1 + R_1}$$

$$D_1^{(2)} = C_1 \cdot \frac{r_1 R_1}{r_1 + R_1} \left[\text{VDD} \cdot \left(\frac{R_1}{r_1 + R_1}\right) - v_1(0)\right]$$

$$D_0^{(2)} = \text{VDD} \cdot C_1 r_1 \left(\frac{R_1}{r_1 + R_1}\right)^2$$

$$\Delta_0^{(2)} = \text{VDD} \cdot C_1 \frac{r_1 R_1}{(r_1 + R_1)^2}$$

$$\Delta^{(2)} = \frac{C_1 r_1}{r_1 + R_1}\left[VDD \cdot \frac{R_1}{r_1 + R_1} - v_1(0)\right] \qquad (9)$$

Theorem 5(b). Given the parameters for network N_n, the parameters for the network N_{n+1} (see Fig. 2(b)) are given by

$$\rho^{(n+1)} = r_n + \frac{R_n \rho^{(n)}}{R_n + \rho^{(n)}}$$

$$v_n^{(n+1)}(\infty) = VDD\left[1 - \frac{r_n}{\rho^{(n+1)}}\right]$$

$$v_i^{(n+1)}(\infty) = \left(\frac{v_n^{(n+1)}(\infty)}{VDD}\right)v_i^{(n)}(\infty)$$

$$\overline{C}^{(n+1)} = v_n^{(n+1)}(\infty)\left[C_n + \frac{\overline{C}^{(n)}}{VDD}\right]$$

$$Q^{(n+1)} = v_n(0)C_n + Q^{(n)}$$

$$\left(R_n^r\right)^{(n+1)} = \frac{1}{1 + \dfrac{r_n}{R_n} + r_n \sigma^{(n)}}$$

$$\left(R_i^r\right)^{(n+1)} = \left(R_i^r\right)^{(n)} \cdot \left(R_n^r\right)^{(n)}$$

$$\sigma^{(n+1)} = \left(R_n^r\right)^{(n+1)} \cdot \left[\sigma^{(n)} + \frac{1}{R_n}\right]$$

$$D_n^{(n+1)} = r_n\left(R_n^r\right)^{(n+1)} \cdot$$
$$\left[\overline{C}^{(n+1)} - Q^{(n+1)} - \Delta^{(n)} - \left(\frac{v_n^{(n+1)}(\infty)}{VDD} - 1\right)\Delta_\delta^{(n)}\right]$$

$$DO_n^{(n+1)} = r_n\left(R_n^r\right)^{(n+1)} \cdot \left[\overline{C}^{(n+1)} - \left(\frac{v_n^{(n+1)}(\infty)}{VDD}\right)\Delta_\delta^{(n)}\right]$$

$$DO_i^{(n+1)} = DO_n^{(n+1)} + \left(\frac{v_n^{(n+1)}(\infty)}{VDD}\right)DO_i^{(n)}$$

$$D_i^{(n+1)} = D_i^{(n)} + DO_i^{(n+1)} - DO_i^{(n)} -$$
$$r_n\left(R_i^r\right)^{(n+1)} \cdot \left(Q^{(n+1)} + \Delta^{(n)} - \Delta_\delta^{(n)}\right)$$

$$\Delta_\delta^{(n+1)} = \frac{\sigma^{(n+1)} \cdot DO_n^{(n+1)}}{\left(R_n^r\right)^{(n+1)}} + \left(\frac{v_n^{(n+1)}(\infty)}{VDD}\right)\Delta_\delta^{(n)}$$

$$\Delta^{(n+1)} = \Delta^{(n)} + \Delta_\delta^{(n+1)} - \Delta_\delta^{(n)} -$$
$$r_n\left(R_n^r\right)^{(n+1)} \cdot \sigma^{(n)}\left[Q^{(n+1)} + \Delta^{(n)} - \Delta_\delta^{(n)}\right] \qquad (10)$$

Theorem 5(c). Given the parameters for networks N_n and N_m, the parameters for the network N_{n+m} (see Fig. 2(c)) are given by

$$\rho^{(n+m-1)} = \frac{\rho^{(n)}\rho^{(m)}}{\rho^{(n)} + \rho^{(m)}}$$

$$v_i^{(n+m-1)}(\infty) = \begin{cases} v_i^{(n)}(\infty), & i = 1,\dots, n-1 \\ v_{i-n+1}^{(m)}(\infty), & i = n,\dots, n+m-2 \end{cases}$$

$$\overline{C}^{(n+m-1)} = \overline{C}^{(n)} + \overline{C}^{(m)}$$

$$Q^{(n+m-1)} = Q^{(n)} + Q^{(m)}$$

$$\left(R_i^r\right)^{(n+m-1)} = \begin{cases} \left(R_i^r\right)^{(n)} & i=1,\dots,n-1 \\ \left(R_{i-n+1}^r\right)^{(m)} & i=n,\dots,n+m-2 \end{cases}$$

$$\sigma^{(n+m-1)} = \sigma^{(n)} + \sigma^{(m)}$$

$$D_i^{(n+m-1)} = \begin{cases} D_i^{(n)} & i=1,\dots,n-1 \\ D_{i-n+1}^{(m)} & i=n,\dots,n+m-2 \end{cases}$$

$$DO_i^{(n+m-1)} = \begin{cases} DO_i^{(n)} & i=1,\dots,n-1 \\ DO_{i-n+1}^{(m)} & i=n,\dots,n+m-2 \end{cases}$$

$$\Delta_\delta^{(n+m-1)} = \Delta_\delta^{(n)} + \Delta_\delta^{(m)}$$
$$\Delta^{(n+m-1)} = \Delta^{(n)} + \Delta^{(m)} \qquad (11)$$

The algorithm for delay computation at a node in an RC network follows immediately from Theorems 5a-c. Starting from all the leaves, build the tree using steps a, b & c as given earlier in this section, until the entire tree has been built. At each stage of construction, update the relevant parameters as given by Theorem 5.
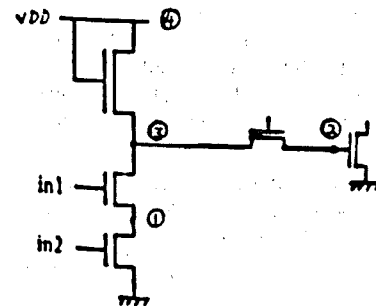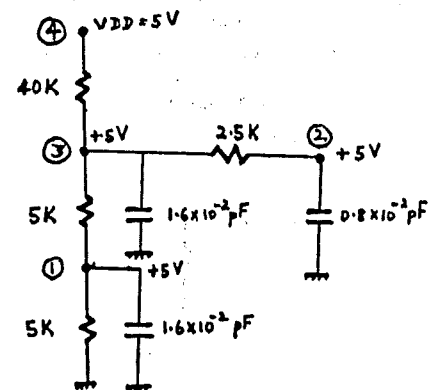

Figure 3(a). A nMOS NAND gate.

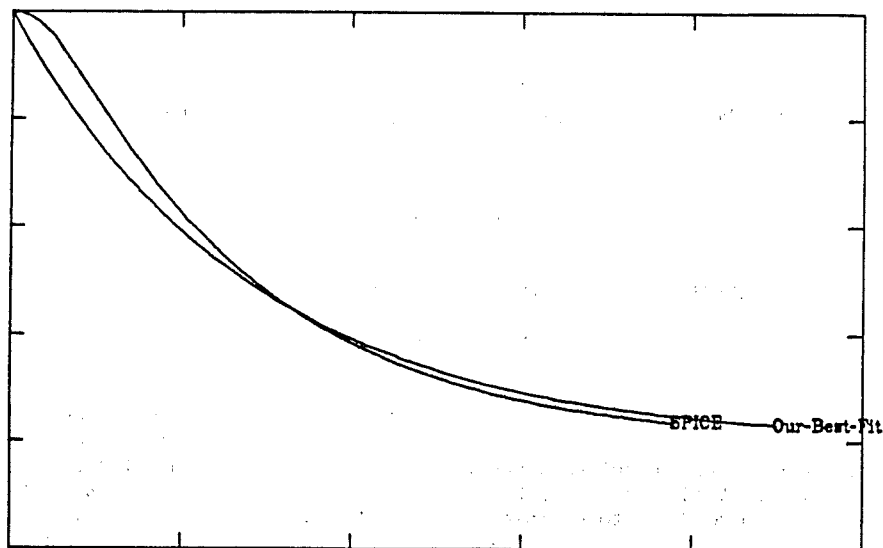Figure 3(b). An RC network for the NAND gate.

Figure 4. The waveforms $v_2(t)$ and $\bar{v}_2(t)$.

6. An Example

Consider the NAND gate shown in Fig. 3(a), with both gate transistors in the 'ON' state. The RC network derived from this is shown in Fig. 3(b).

Fig. 4 shows a plot of the "best fit" waveform of $v_2(t)$. Also plotted in the same figure is the waveform obtained by a SPICE simulation of the RC circuit.

The waveform obtained by our analysis follows the SPICE waveform very closely, although it is a single time constant approximation.

7. Conclusions

An expression for delay, based upon the delay of Elmore, has been derived for RC trees with charge sharing or leaky capacitors. Our definition of delay provides a "best fit" exponential waveform in networks with charge sharing, with more than one source and with nonideal capacitors. We are currently examining the use of these networks in ELOGIC [6].

An important fact to keep in mind when using our results is that we have provided a "best fit" single exponential for the linear RC model. A simulation program like SPICE can handle nonlinear circuits, although much more slowly. Thus, an interesting topic for future research is to study the effects of linearization and the speed vs. accuracy tradeoffs in simulation programs.

We also need to study the usefulness of bounding the waveforms of a nonlinear circuit by waveforms derived from a linear circuit, and, if found useful, derive tight lower and upper bounds on the waveform. One important step in this direction is the derivation of bounding waveforms for linear circuits [9, 11, 12].

Our current research effort is to extend our results to RC networks with floating capacitances, in order to model the important "Miller effect".

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